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09/788,282	02/16/2001	Michele Borgatti	854063.616	5300

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EXAMINER	
FAULK, DEVONA E	
ART UNIT	**PAPER NUMBER**
2615	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/788,282	BORGATTI ET AL.	
	Examiner	Art Unit	
	Devona E. Faulk	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 January 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11 and 15-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11 and 15-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 February 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Remarks

1. Applicant's arguments, filed 1/23/2008, with respect to the 112 1st rejection of claim 1 have been fully considered and are persuasive. The 112 1st rejection of claim 1 has been withdrawn. The applicant has directed the examiner to page 4 in the specification which discloses the claim language " the control unit being structured to provide a user interface to a user via an external user device" of claim 1.

2. The applicant has cancelled claims 12-14 and 23-25.

3. Upon further consideration, the examiner has determined that the claims can be rejected in view of Kaufman.

Claim Objections

4. Claims 1 and 15 are objected to because of the following informalities: Claims 1 and 15 recite " a non-volatile memory.... generating said second stream of compressed digital signals". The specification discloses on page 6, lines 1-29 that the memory device receives and stores a second stream of compressed digital signals according to control signals generated by the control unit. Appropriate correction is required. The examiner has interpreted the language as " a non-volatile memory...storing said second stream of compressed digital signals".

Specification

5. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: Claims 1 and 15 recite " a non-volatile

memory.... generating said second stream of compressed digital signals". The specification discloses on page 6, lines 1-29 that the memory device receives and stores a second stream of compressed digital signals according to control signals generated by the control unit. The examiner has interpreted the language as " a non-volatile memory...storing said second stream of compressed digital signals.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Walters et al. (US 6,453,281) in view of Kaufman (US 6,251,048).

Regarding claim 1, Walters discloses an electronic device for the recording/reproduction of voice data, comprising:

A main transmission line (internal bus, Figure 4);

A control unit coupled to said main transmission line, the control unit being structured to provide a user interface to a user via an external user interface device (CPU 120, Figure 4 is coupled to the internal bus and provides an user interface 128 via an external user interface; column 7, line 60- column 8, line 8);

A signal-conversion unit connected to said main transmission line, said signal conversion unit (codec 158, Figure 4 is connected to the internal bus 128; column 8,line 60-65) comprising:

reception means for receiving an input analog signal correlated to a voice signal (codec 158 receives an input analog signal from microphone 46; column 8, lines 63-66)

,

compression means for compressing said input analog signal and generating a first stream of compressed digital signals (a compression means is implicit because codec 158 codes signals received from the microphone to a compressed format and the compressed digital signals are stored in memory unit 122; column 8, line 64-column 9, line 5),

fetching means for receiving a second stream of compressed digital signals, and decompression means for decompressing said second stream of compressed digital signals and generating an output analog signal (audio stored in the memory of the CPU 120, which reads on second stream of compressed digital signals, may be coded by the codec 158 prior to transmitting the information to an external device; column 9, lines 6-9; fetching means is therefore implicit and it is obvious that decompression would occur before the audio is transmitted to an external device) ; and

a non-volatile memory unit integrated in said chip and connected to said main transmission line, said non-volatile memory unit storing said first stream of compressed digital data in memory locations, and storing said second stream of compressed digital data according to first control signals generated by said control unit (Flash memory 122 received compressed digital data from the codec, column 8, line 63-column 9, line 3, this reads on first and second stream of compressed digital data);

and a memory unit interface coupled between the non-volatile memory unit and said main transmission line, the memory unit interface being structured to coordinate exchange of data and instructions (implicitly some interface that coordinates exchange of data and instructions between the non-volatile unit and said main transmission line).

Walters fails to disclose that the control unit, memory unit, signal conversion unit and transmission line are integrated in a single chip. The concept of single-chip voice recorders are known in the art as taught by Kaufman (column 15, lines 59-63).

It would have been obvious to one of ordinary skill in the art have all the components onto a single-chip for the purpose of reducing the size of the device.

Regarding claim 2, Walters as modified discloses wherein said control unit further comprises a microprocessor (CPU 120 reads on microprocessor).

Regarding claim 3, Walters as modified discloses wherein said control unit further comprises a microcontroller (CPU 120 reads on microcontroller).

8. Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Walters et al. (US 6,453,281) in view of Kaufman (US 6,251,048) in further view of Unno et al. (6,076,063).

Regarding claim 4, Walters as modified discloses a signal conversion unit which inherently has a converter circuit. Walters as modified fails to disclose a temporary storage means coupled to said converter circuit for temporarily storing said first stream and said second stream of compressed digital signals. Unno et al. et al taught an

audio player and recorder having a buffer memory 6 which temporarily stores data received from the compressor 4 (first stream) and data read from the flash memory 8 (second stream)(column 5, lines 14-17). The buffer memory is coupled to a converter circuit. It would have been obvious to one of ordinary skill in the art to modify Walters as modified to have the signal conversion unit include a buffer memory for the benefit of providing quick temporary access to data.

Regarding claim 5, Walters as modified fails to disclose that the converter circuit further comprises dividing means for generating blocks of digital signals having a fixed dimension, each of said blocks of digital signals comprising one portion of a pre-set duration of said voice signal. Unno et al. et al taught that the compression means generates blocks of digital samples having a fixed dimension in column 7, lines 30-35). It would have been obvious to modify Walters as modified to have the converter comprise a dividing means as claimed in order to enable faster processing. .

9. Claims 6,7 and 15-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Walters et al. (US 6,453,281) in view of Kaufman (US 6,251,048) in further view of Unno et al. (6,076,063) in further view of Daberko (5,787,445)

Regarding claim 6, Walters as modified discloses a temporary storage means. Walters as modified fails to disclose that the temporary storage means comprises a first memory buffer and a second memory buffer, and in that said signal-conversion unit further comprises control means for controlling transfer of said blocks of digital signals alternately to said first memory buffer and said second memory buffer according to

second control signals supplied by said control unit. Daberko teaches a non-volatile memory (flash) having first and second memory buffers in figure 3C. As suggested in column 9 lines 44-55, it was advantageous to allow the buffers to switch tasks. One memory buffer can be disseminated or unloaded while the other memory buffer is written to primary memory. A control means is implicit. Therefore, it would have been obvious to modify Walters as modified by one incorporating first and second memory buffers for the benefit of being able to readily switch tasks.

Regarding claim 7, the examiner takes Official Notice that it was well known to use RAM as memory buffers. . It would have been obvious to modify Walters as modified by using RAM type memory for the memory buffers so that data can be accessed at any time and in any order.

Regarding claim 15, Walters discloses an electronic device for the recording/reproduction of voice data, comprising:

A main transmission line (internal bus, Figure 4);

A control unit coupled to said main transmission line, the control unit being structured to provide a user interface to a user via an external user interface device (CPU 120, Figure 4 is coupled to the internal bus and provides an user interface 128 via an external user interface; column 7, line 60- column 8, line 8);

A signal-conversion unit connected to said main transmission line, said signal conversion unit (codec 158, Figure 4 is connected to the internal bus 128; column 8,line 60-65), said signal conversion unit receiving an input analog signal correlated to an

analog voice signal (codec 150 receives analog signal from microphone 46; column 8, lines 63-66) and including:

A converter circuit coupled to received said input analog signal and operating a compression/decompression algorithm that compresses said input analog signal and generates a first stream of compressed digital signals, and decompresses a second stream of compressed digital signals and generates and output analog signal (implicit; codec 158 codes signals received from the microphone to a compressed format and the compressed digital signals are stored in memory unit 122; column 8, line 64-column 9, line 5 and audio stored in the memory of the CPU 120, which reads on second stream of compressed digital signals, may be coded by the codec 158 prior to transmitting the information to an external device; column 9, lines 6-9; it is obvious that decompression would occur before the audio is transmitted to an external device);

a non-volatile memory unit integrated in said chip and connected to said main transmission line, said non-volatile memory unit storing said first stream of compressed digital data in memory locations, and storing said second stream of compressed digital data according to first control signals generated by said control unit (Flash memory 122 received compressed digital data from the codec, column 8, line 63-column 9, line 3, this reads on first and second stream of compressed digital data);

and a memory unit interface coupled between the non-volatile memory unit and said main transmission line, the memory unit interface being structured to coordinate exchange of data and instructions (implicitly some interface that coordinates exchange of data and instructions between the non-volatile unit and said main transmission line).

Walters fails to disclose that the control unit, memory unit, signal conversion unit and transmission line are integrated in a single chip. The concept of single-chip voice recorders are known in the art as taught by Kaufman (column 15, lines 59-63).

It would have been obvious to one of ordinary skill in the art have all the components onto a single-chip for the purpose of reducing the size of the device.

Walters as modified fails to disclose that the signal conversion unit includes first and second memory buffers to sequentially receive said first and second streams of compressed digital signals.

Unno et al. discloses an audio player and recorder having a buffer memory 6 which temporarily stores data received from the compressor 4 (first stream) and data read from the flash memory 8 (second stream)(column 5, lines 14-17). The buffer memory is coupled to a converter circuit. It would have been obvious to one of ordinary skill in the art to modify Walters as modified to have the signal conversion unit include a buffer memory for the benefit of providing quick temporary access to data.

Walters as modified discloses a temporary storage means. Walters as modified fails to disclose that the temporary storage means comprises a first memory buffer and a second memory buffer, and in that said signal-conversion unit further comprises control means for controlling transfer of said blocks of digital signals alternately to said first memory buffer and said second memory buffer according to second control signals supplied by said control unit. Daberko teaches a non-volatile memory (flash) having first and second memory buffers in figure 3C. As suggested in column 9 lines 44-55, it was

advantageous to allow the buffers to switch tasks. One memory buffer can be disseminated or unloaded while the other memory buffer is written to primary memory. Therefore, it would have been obvious to modify Walters as modified by one incorporating first and second memory buffers for the benefit of being able to readily switch tasks.

Regarding claim 16, Walters as modified discloses that the converter circuit further comprises dividing means for generating blocks of digital signals having a fixed dimension, each of said blocks of digital signals comprising one portion of a pre-set duration of said voice signal. Unno et al. et al taught that the compression means generates blocks of digital samples having a fixed dimension in column 7, lines 30-35).

Regarding claim 17, Walters as modified discloses that the signal conversion unit comprises a control circuit, said control circuit controlling transfer of blocks of digital signals alternately to said first memory buffer and said second memory buffer according to second control signals supplied by said control unit. Daberko teaches a non-volatile memory (flash) having first and second memory buffers in figure 3C. As suggested in column 9 lines 44-55, it was advantageous to allow the buffers to switch tasks. One memory buffer can be disseminated or unloaded while the other memory buffer is written to primary memory. A control circuit is implicit. All elements of claim 17 are comprehended by the rejection of claims 15 and 16.

Regarding claim 18, the examiner takes Official Notice that it was well known to use RAM as memory buffers. It would have been obvious to modify Walters as modified

by using RAM type memory for the memory buffers so that data can be accessed at any time and in any order.

10. . Claims 9 –11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Walters et al. (US 6,453,281) in view of Kaufman (US 6,251,048) in further view Ogawa (6,604,168).

Regarding claim 9, Walters as modified discloses a non-volatile unit. Walters as modified fails to disclose that the non-volatile memory included a memory device having a first memory area storing digital signals and a second memory area containing information regarding occupation of memory locations of the first memory area. Ogawa discloses a flash EEPROM management system. The system has a flash ROM 15 having a management area and data area for storing digital signals. See figures 4 and 5a-c. As discussed in the "Summary of the Invention" section, column 2,lines 20-57, the management area stores state information indicating whether a corresponding data area is used, unused or busy. Thus, it was well known to have a memory containing data signals and information regarding occupation (used/unused flags) of the memory locations containing data signals. Therefore, it would have been obvious to modify Walters as modified by incorporation the teachings of Ogawa for the benefit of better data management.

Regarding claim 10, . Walters as modified discloses a first sub-area (the first sub-area is the used state flag 156 and it is inherent that another sub-area contains read-

sequence pointers). All elements of claim 10 are comprehended by the rejection of claim 9.

Regarding claim 11, the examiner takes official notice is taken that the use and advantages of multi-level flash EEPROMS were notoriously well known in the art of digital signal storage and one of ordinary skill in the art would have been motivated to use them for the benefit of providing storage even when power has been removed.

11. Claims 8 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Walters et al. (US 6,453,281) in view of Kaufman (US 6,251,048) in further view of Unno et al. (6,076,063) in further view of Daberko (5,787,445) in further view of Rossum.

Regarding claim 8, Walters as modified fails to disclose that the control means further comprises: means for transferring first blocks of digital signals to said first memory buffer; first means for detecting filling of said first memory buffer; first transfer-switching means for transferring second blocks of digital signals to said second memory buffer and for sending said first blocks of digital signals to said non-volatile memory unit; second means for detecting filling of said second memory buffer; and second transfer-switching means for transferring third blocks of digital signals to said first memory buffer and for sending said second blocks of digital signals to said non-volatile memory unit. This is known as "ping-pong" buffering. This feature was well known in the art, as evidenced by Rossum. Column 1 lines 12-26 discloses the art of ping-pong buffering noting that when a first buffer is full then a second buffer is filled and the data from the first buffer is processed. This process is repeated when the second buffer is full and

control is passed back to the first buffer. Thus, there was taught alternating between two buffers and detecting filling of each of the buffers. The buffers were examined to see if they were full since control is passed to the other buffer when one is full. It would have been obvious to one of ordinary skill in the art at the time of invention to use the feature of "ping-pong" buffering for the benefit of speeding up the processing.

Regarding claim 19, Walters as modified fails to disclose that the control circuit further comprises: transferring means for transferring first blocks of digital signals to said first memory buffer; first detecting means for detecting filling of said first memory buffer; first transfer-switching means for transferring second blocks of digital signals to said second memory buffer and for sending said first blocks of digital signals to said non-volatile memory unit; second detecting means for detecting filling of said second memory buffer; and second transfer-switching means for transferring third blocks of digital signals to said first memory buffer and for sending said second blocks of digital signals to said non-volatile memory unit. This is known as "ping-pong" buffering. This feature was well known in the art, as evidenced by Rossum. Column 1 lines 12-26 discloses the art of ping-pong buffering noting that when a first buffer is full then a second buffer is filled and the data from the first buffer is processed. This process is repeated when the second buffer is full and control is passed back to the first buffer. Thus, there was taught alternating between two buffers and detecting filling of each of the buffers. The buffers were examined to see if they were full since control is passed to the other buffer when one is full. It would have been obvious to one of ordinary skill in

the art at the time of invention to use the feature of "ping-pong" buffering for the benefit of speeding up the processing.

12. Claims 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Walters et al. (US 6,453,281) in view of Kaufman (US 6,251,048) in further view of Unno et al. (6,076,063) in further view of Daberko (5,787,445) in further view Ogawa (6,604,168).

Regarding claim 20, Walters as modified discloses a non-volatile unit. Walters as modified fails to disclose that the non-volatile memory included a memory device having a first memory area storing digital signals and a second memory area containing information regarding occupation of memory locations of the first memory area. Ogawa discloses a flash EEPROM management system. The system has a flash ROM 15 having a management area and data area for storing digital signals. See figures 4 and 5a-c. As discussed in the "Summary of the Invention" section, column 2, the management area stores state information indicating whether a corresponding data area is used, unused or busy. Thus, it was well known to have a memory containing data signals and information regarding occupation (used/unused flags) of the memory locations containing data signals. Therefore, it would have been obvious to modify Walters as modified by incorporation the teachings of Ogawa for the benefit of better data management.

Regarding claim 21, . Walters as modified discloses a first sub-area (the first sub-area is the used state flag 156 and it is inherent that another sub-area contains

read-sequence pointers). All elements of claim 10 are comprehended by the rejection of claim 9.

Regarding claim 22, the examiner takes official notice is taken that the use and advantages of multi-level flash EEPROMS were notoriously well known in the art of digital signal storage and one of ordinary skill in the art would have been motivated to use them for the benefit of providing storage even when power has been removed.

. ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Devona E. Faulk whose telephone number is 571-272-7515. The examiner can normally be reached on 8 am - 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vivian Chin can be reached on 571-272-7848. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Devona E. Faulk/
Examiner
Art Unit 2615
2/29/2008

VIVIAN CHIN
SUPERVISORY PATENT EXAMINER